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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,665	NGUYEN ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8,16,17 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,16,17 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 4-8, 16-17, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Goodman et al. (U.S. Patent No. 6,282,601) with Smith et al (U.S. Patent No. 3,643,227) or Inoue (U.S. Patent No. 4,954,945), or over the combination of the Tyner et al. (U.S. Patent No. 6,272,618) with Smith or Inoue.

Referring to claim 1: Tyner discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature to a predetermined register of the first processor (the program counter disclosed in column 4, lines 41-42); executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 3, line 37); receiving

at each processor an instruction that a software system management interrupt has been issued (figure 2, steps 102-106); entering system management mode at each processor (figure 2, step 104); saving the register contents of each processor to a memory space associated with each respective processor (figure 2, step 106); scanning the contents of the memory space associated with each processor (column 4, lines 40-42); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 3,steps 130, 132).

Goodman discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature (the identifying signature disclosed in column 2, line 15, and figure 3, step 104) to a predetermined register of the first processor; executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 1, line 29); receiving at each processor an instruction that a software system management interrupt has been issued (figure 3, step 106); entering system management mode at each processor; saving the register contents of each processor to a memory space associated with each respective processor (figure 3, step 106); selecting a second processor as the system management interrupt handler (column 1, lines 46-49); scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined

signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman explicitly discloses that the SMI is to be routed to a designated processor for handling (column 1, lines 48-49).

Neither Tyner nor Goodman explicitly discloses or teaches selecting a processor among the plurality of the processors to handle the task according to an arbitration scheme. Smith discloses that it is known to control each processor's operations by monitoring it and to assign a job thereto when the processor is found to be idle (abstract). Inoue discloses that it is known to select a processor, which can best execute a requested task (abstract). Hence, it would have been obvious at the time Applicant made the invention to one having ordinary skill in the computer art to adopt either Smith or Inoue's teaching to either Tyner or Goodman because Inoue enables the system to operate efficiently without beforehand programming in the case of changing number of the processor (column 1, lines 45-59), and Smith enables the system to operate optimally by assigning the job in a flexible manner (column 1, lines 69-75).

Referring to claim 4: Claim 1's argument applies; furthermore, Tyner discloses locating the processor, which causes the interrupt (column 4, lines 33-34, figure 3, step 120). In addition, since Smith teaches one to select the idle processor, it can be any processor, including the one just causes the SMI.

Referring to claim 5: Claim 1's argument applies; Tyner discloses that the processor writes to the memory (figure 1, structure 18) via the chip set's port (figure 1, structure 16). Goodman discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18). Furthermore, Applicant also discloses the processors' access

to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9).

Referring to claim 6: Claim 5's argument applies; furthermore, both Tyner and Goodman's chip sets are a PCI bridge.

Referring to claim 7: Claim 5's argument applies; furthermore, Tyner discloses an expansion bridge (figure 1, structure 42) and Goodman discloses an expansion bridge (figure 1, structure 50).

Referring to claim 8: Claim 7's argument applies; furthermore, Tyner discloses that each of the processors of the system to enter system management mode (column 4, lines 9-10), and Goodman also discloses that each of the processors of the system to enter system management mode (column 1, lines 50-54).

Referring to claim 16: Claim 16 is rejected as the claim 1's argument above. Tyner discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature to a predetermined register of the first processor (the program counter disclosed in column 4, lines 41-42); executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 3, line 37); receiving at each processor an instruction that a software system management interrupt has been issued (figure 2, steps 102-106); entering system management mode at each processor (figure 2, step 104); saving the register contents of each processor to a memory space associated with each respective processor (figure 2, step 106); scanning the contents of the memory space associated with each processor (column 4, lines 40-42); and when the second processor locates the saved predetermined signature in one of the

memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 3,steps 130, 132).

Goodman discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature (the identifying signature disclosed in column 2, line 15, and figure 3, step 104) to a predetermined register of the first processor; executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 1, line 29); receiving at each processor an instruction that a software system management interrupt has been issued (figure 3, step 106); entering system management mode at each processor; saving the register contents of each processor to a memory space associated with each respective processor (figure 3, step 106); selecting a second processor as the system management interrupt handler (column 1, lines 46-49); scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman explicitly discloses that the SMI is to be routed to a designated processor for handling (column 1, lines 48-49).

Neither Tyner nor Goodman explicitly discloses or teaches selecting a processor among the plurality of the processors to handle the task according to an arbitration scheme. Smith discloses that it is known to control each processor's operations by monitoring it and to assign a

job thereto when the processor is found to be idle (abstract). Inoue discloses that it is known to select a processor, which can best execute a requested task (abstract). Hence, it would have been obvious at the time Applicant made the invention to one having ordinary skill in the computer art to adopt either Smith or Inoue's teaching to either Tyner or Goodman because Inoue enables the system to operate efficiently without beforehand programming in the case of changing number of the processor (column 1, lines 45-59), and Smith enables the system to operate optimally by assigning the job in a flexible manner (column 1, lines 69-75).

Referring to claim 17: Claim is rejected as the claim 4's argument stated above.

Referring to claim 19: Claim 16's argument applies; furthermore, claim 19 is rejected over the claim 5's argument.

Referring to claim 20: Claim 19's argument applies; furthermore, claim 20 is rejected over the claim 6's argument.

Referring to claim 21: Claim 19's argument applies; furthermore, claim 21 is rejected over the claim 7's argument.

Referring to claim 22: Tyner discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature to a predetermined register of the first processor (the program counter disclosed in column 4, lines 41-42); executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 3, line 37); receiving at each processor an instruction that a software system management interrupt has been issued (figure 2, steps 102-106); entering system management mode at each processor (figure 2, step 104); saving the register contents of each processor to a memory space associated with each

respective processor (figure 2, step 106); scanning the contents of the memory space associated with each processor (column 4, lines 40-42); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 3,steps 130, 132).

Goodman discloses a method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature (the identifying signature disclosed in column 2, line 15, and figure 3, step 104) to a predetermined register of the first processor; executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt (column 1, line 29); receiving at each processor an instruction that a software system management interrupt has been issued (figure 3, step 106); entering system management mode at each processor; saving the register contents of each processor to a memory space associated with each respective processor (figure 3, step 106); selecting a second processor as the system management interrupt handler (column 1, lines 46-49); scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman explicitly discloses that the SMI is to be routed to a designated processor for handling (column 1, lines 48-49).

Neither Tyner nor Goodman explicitly discloses or teaches selecting a processor among the plurality of the processors to handle the task according to an arbitration scheme. Smith discloses that it is known to control each processor's operations by monitoring it and to assign a job thereto when the processor is found to be idle (abstract). Inoue discloses that it is known to select a processor, which can best execute a requested task (abstract). Hence, it would have been obvious at the time Applicant made the invention to one having ordinary skill in the computer art to adopt either Smith or Inoue's teaching to either Tyner or Goodman because Inoue enables the system to operate efficiently without beforehand programming in the case of changing number of the processor (column 1, lines 45-59), and Smith enables the system to operate optimally by assigning the job in a flexible manner (column 1, lines 69-75).

Referring to claim 23: Claim is rejected as the claim 4's argument stated above.
Referring to claim 24: Claim 23's argument applies; furthermore, claim 24 is rejected over the claim 5's argument.

Response to Arguments

4. In response to Applicant's argument that Smith and Inoue do not disclose or teach selecting from among a set of processors operable to handle a system management interrupt (Remark, page 11, paragraph 3): As the Office Action states, both Tyner and Goodman disclose the processor(s) operable to handle system management interrupt, but they do not discloses the selecting means to select a processor. Both Smith and Inoue disclose that it is known to select one processor among a plurality of processors to handle the task. Thus, the combination of the

prior arts discloses the selecting from among a set of processors operable to handle a system management interrupt.

5. In response to Applicant's argument that Goodman teaches away from the claimed invention by disclosing that all system management interrupts are to be handled by a single dedicated processor; and Applicant further argues that modifying Goodman would result in distortion of Goodman (Remark, pages 11-12, paragraph 4): Goodman does not teaches away from the claimed invention. Either Smith or Inoue cures the deficiency of the selecting means in the Goodman. The modification of the dedicated processor in the Goodman does not distort Goodman from its processing functionalities. The addition of the selecting means taught by the Smith and Inoue enhanced the processing resource utilization.

6. In response to Applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

7. In response to Applicant's argument that the Tyner's selecting means is not to select a processor to handle the task: The Office Action above is revised accordingly.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 703-305-4571. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-308-3110. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin King
August 30, 2004

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